Mach-RT: A Many Chip Architecture for Ray Tracing

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More Chips! Handle it!

- Higher framerates
- Lower energy

Ray Tracing Performance

- No predictable memory access pattern
  - Is unlike Raster which is able to leverage streaming
- Large energy and time overheads due to irregular DRAM accesses

Previous Work

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- Coalescing memory access
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- Batching and packets for scheduling
  - [Myungbae 2017], [Boulos et al. 2007]
- Ordered ray generation and sorting
  - [Eisenacher et al. 2013], [Purcell et al. 2002]

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- Better data layout
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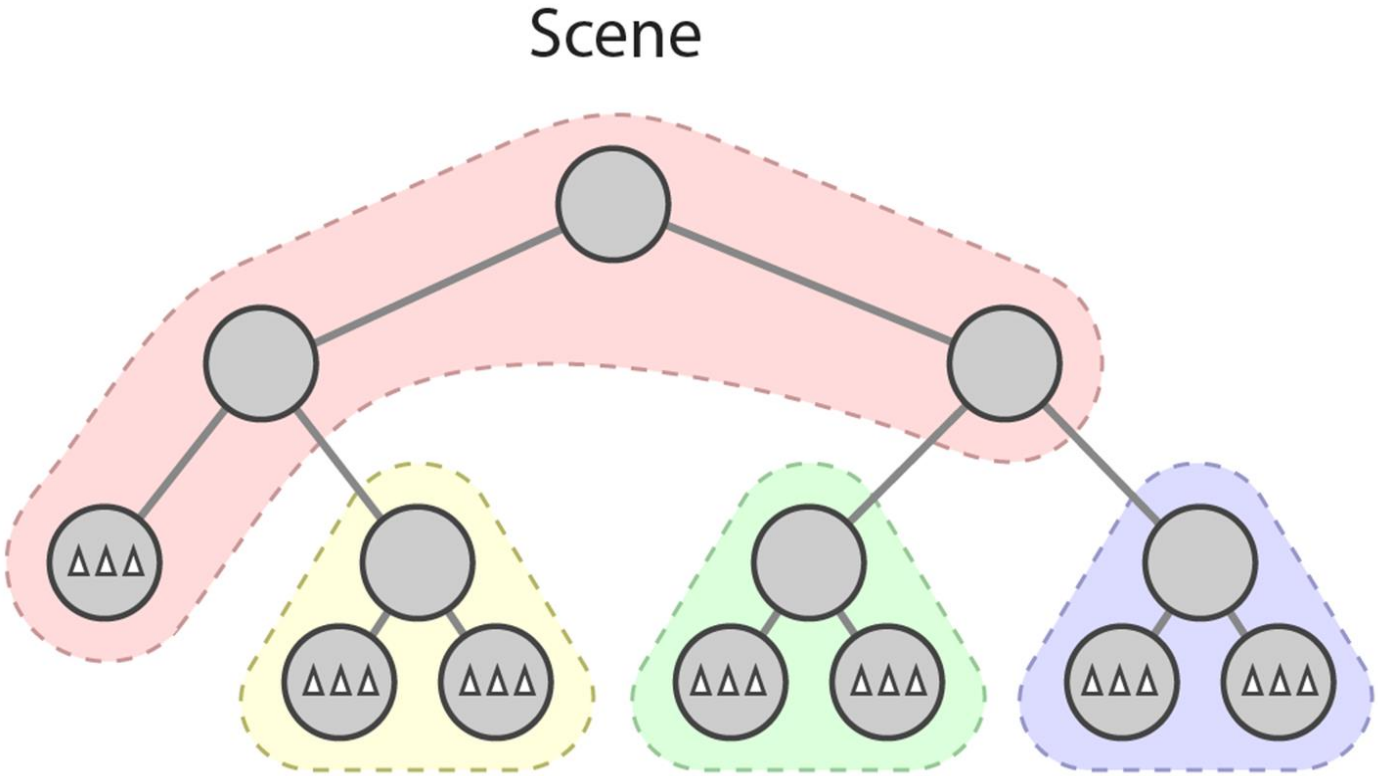
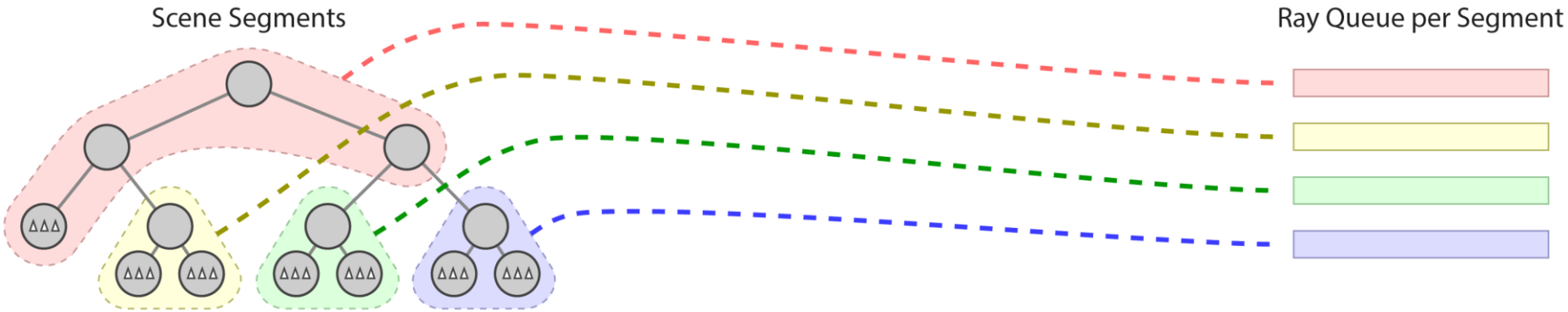
- Compression
  - [Keely 2014], [Ylitie et al. 2017], [Benthin et al. 2018]

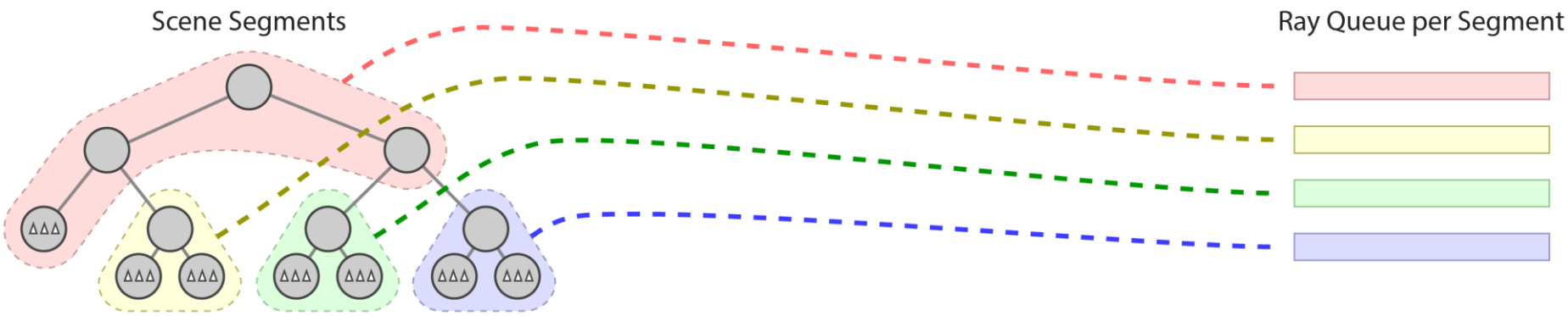
Dual Streaming



Traversal Order

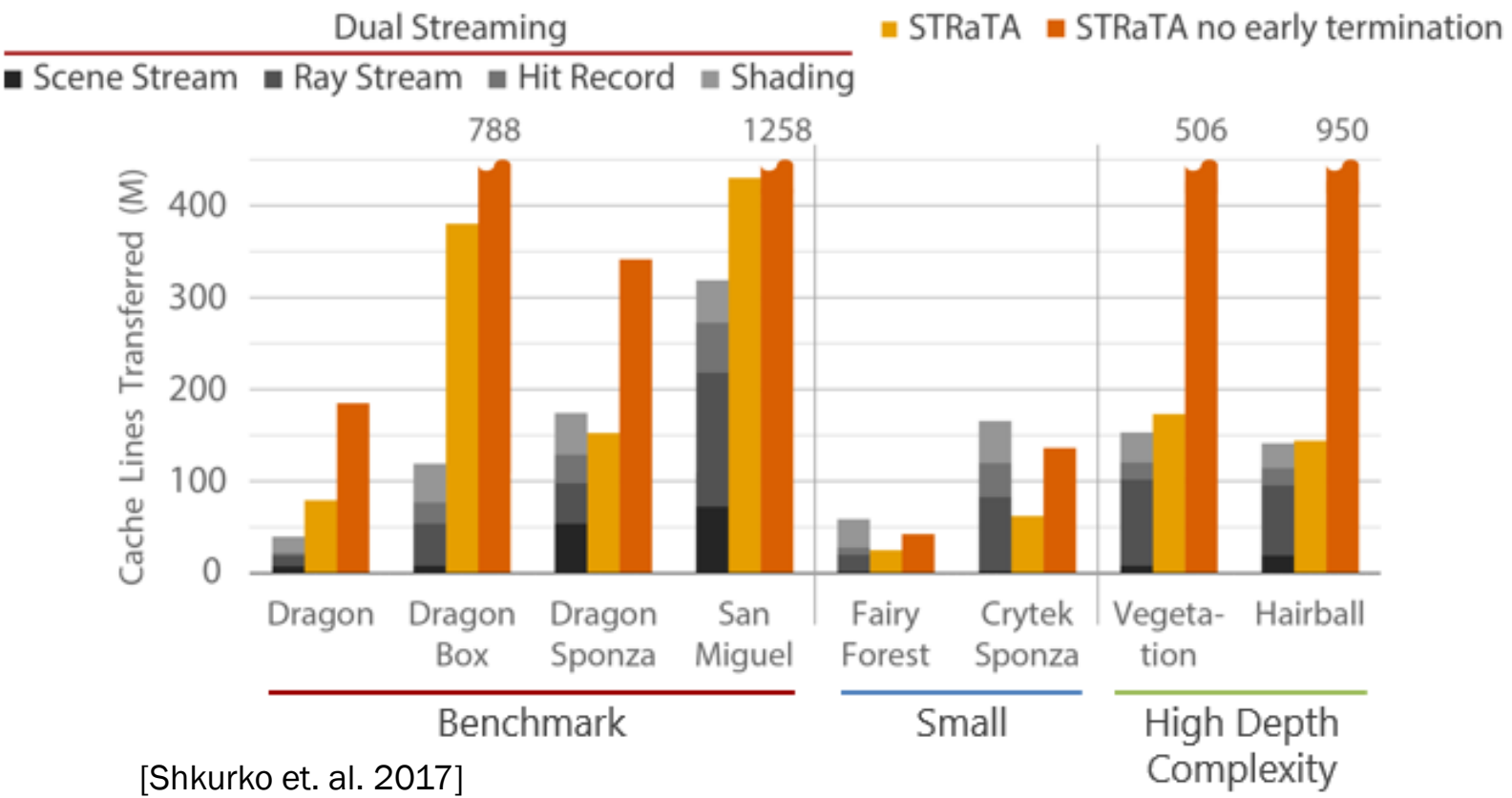


Drawbacks



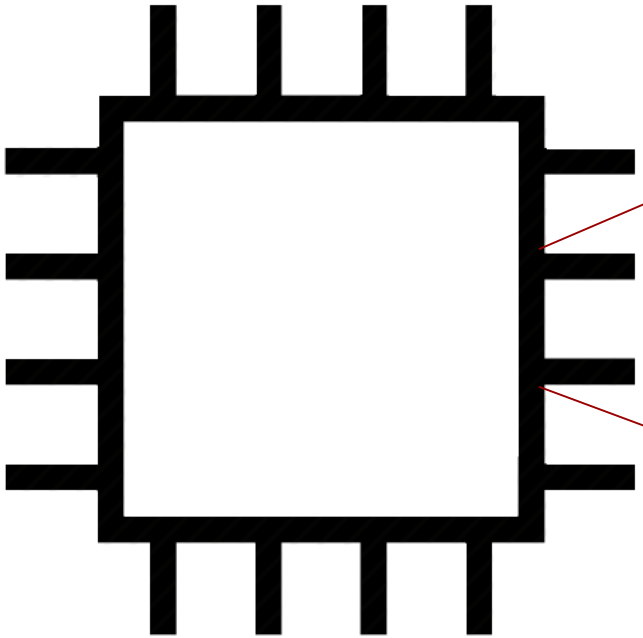
- ✗ Ray Duplication
- ✗ Early Termination

Memory Traffic

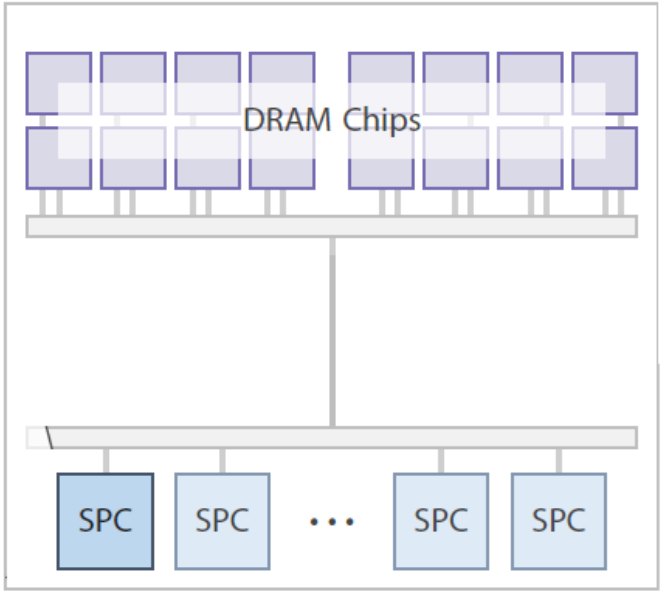


[Shkurko et. al. 2017]

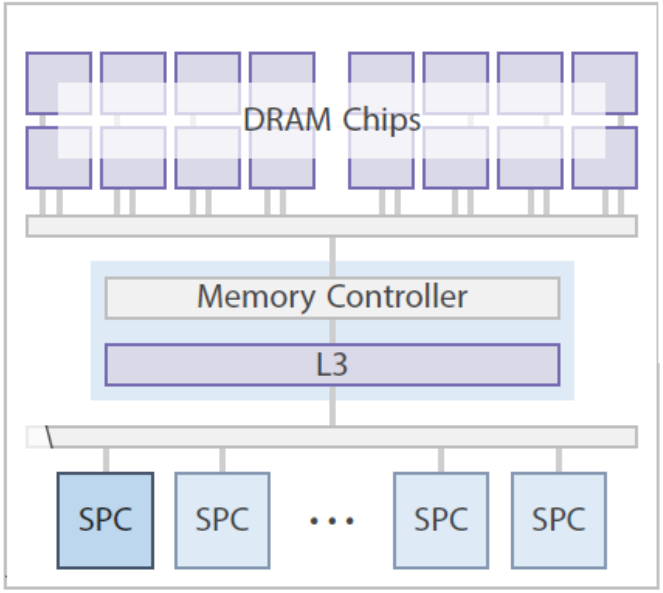
Single Large Chip



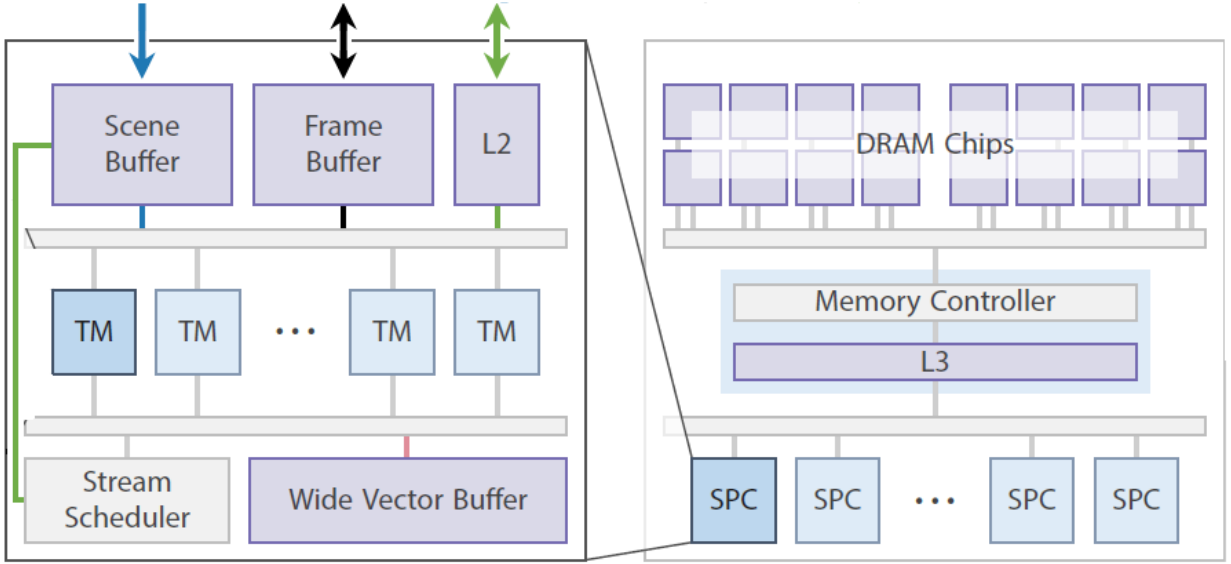
Board of Chips



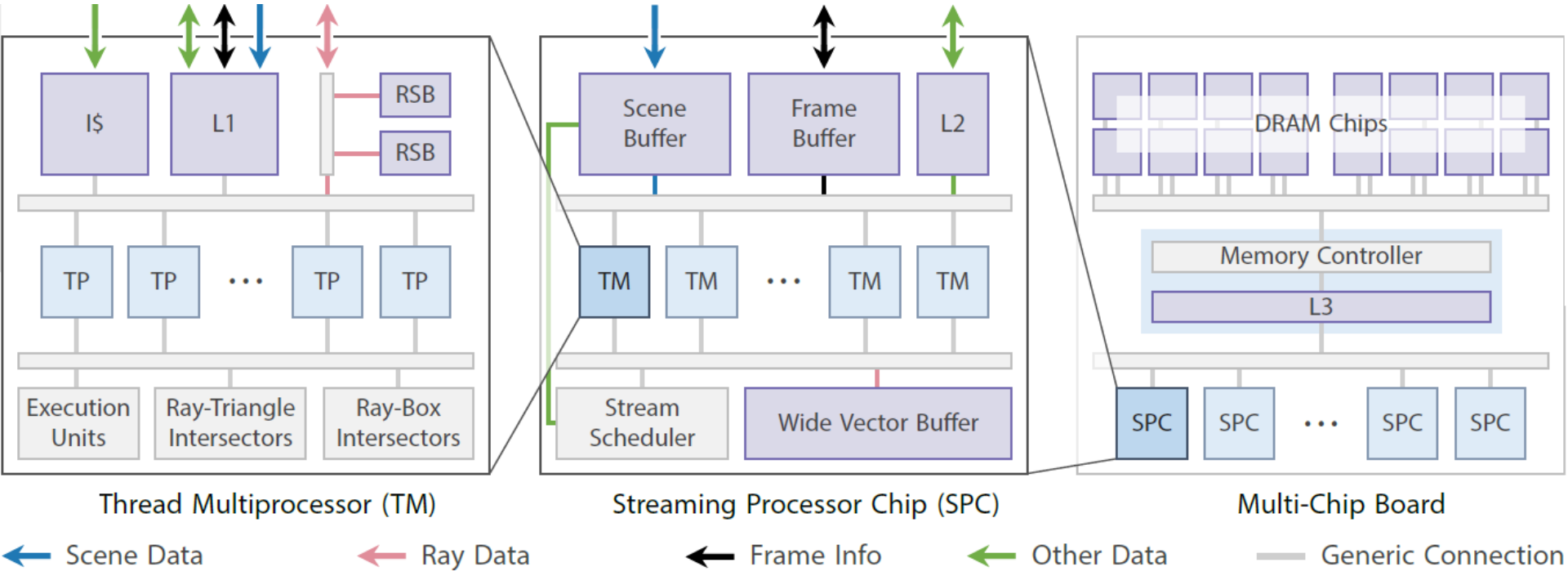
Board of Chips



SPC


Scene Buffer
Frame Buffer
L2
TM
TM
TM
TM
Stream Scheduler
Wide Vector Buffer
DRAM Chips
Memory Controller
L3
SPC
SPC
SPC
SPC
Streaming Processor Chip (SPC)
Multi-Chip Board
Scene Data
Ray Data
Frame Info
Other Data
Generic Connection

Board Final


I$
L1
RSB
RSB
TP
TP
TP
TP
Execution Units
Ray-Triangle Intersectors
Ray-Box Intersectors
Scene Buffer
Frame Buffer
L2
TM
TM
TM
TM
Stream Scheduler
Wide Vector Buffer
DRAM Chips
Memory Controller
L3
SPC
SPC
SPC
SPC
Thread Multiprocessor (TM)
Streaming Processor Chip (SPC)
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Pixel Distribution

- Interleaved pixel assignment

1	2	3	4	1	2
3	1	2	3	4	1
2	3	4	1	2	3
4	1	2	3	4	1
2	3	4	1	2	3
4	1	2	3	4	1

Improvements

- Because of on chip rays:
  - Eliminate ray traffic to DRAM

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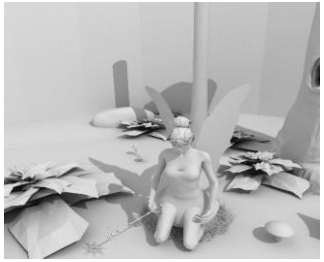
  - Early Ray Termination

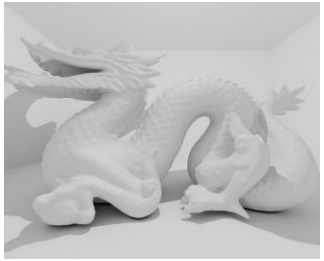
Results

Fairy Forest
174K



Crytek Sponza
262K

Dragon Box
870K



Vegetation
1.1M

Dragon Sponza
6.6M

San Miguel
10.5M

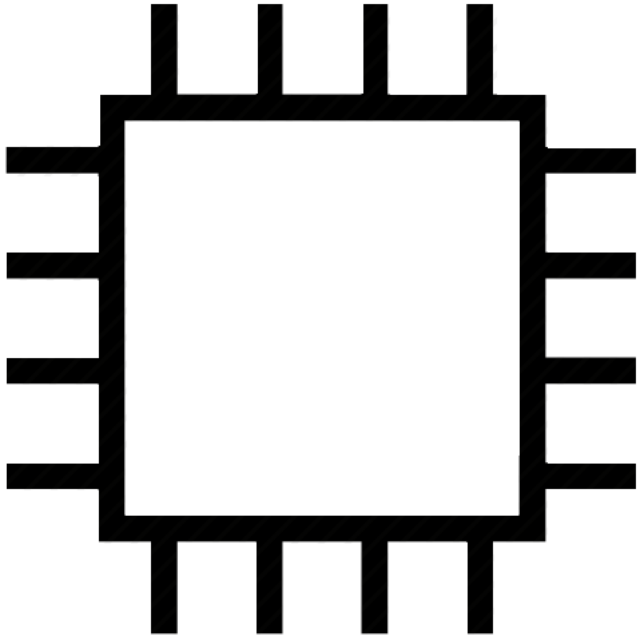
Hardware Simulation

- Cycle accurate simulator
  - Render to frame completion
- Large simulation times
  - Milliseconds of simulated behavior

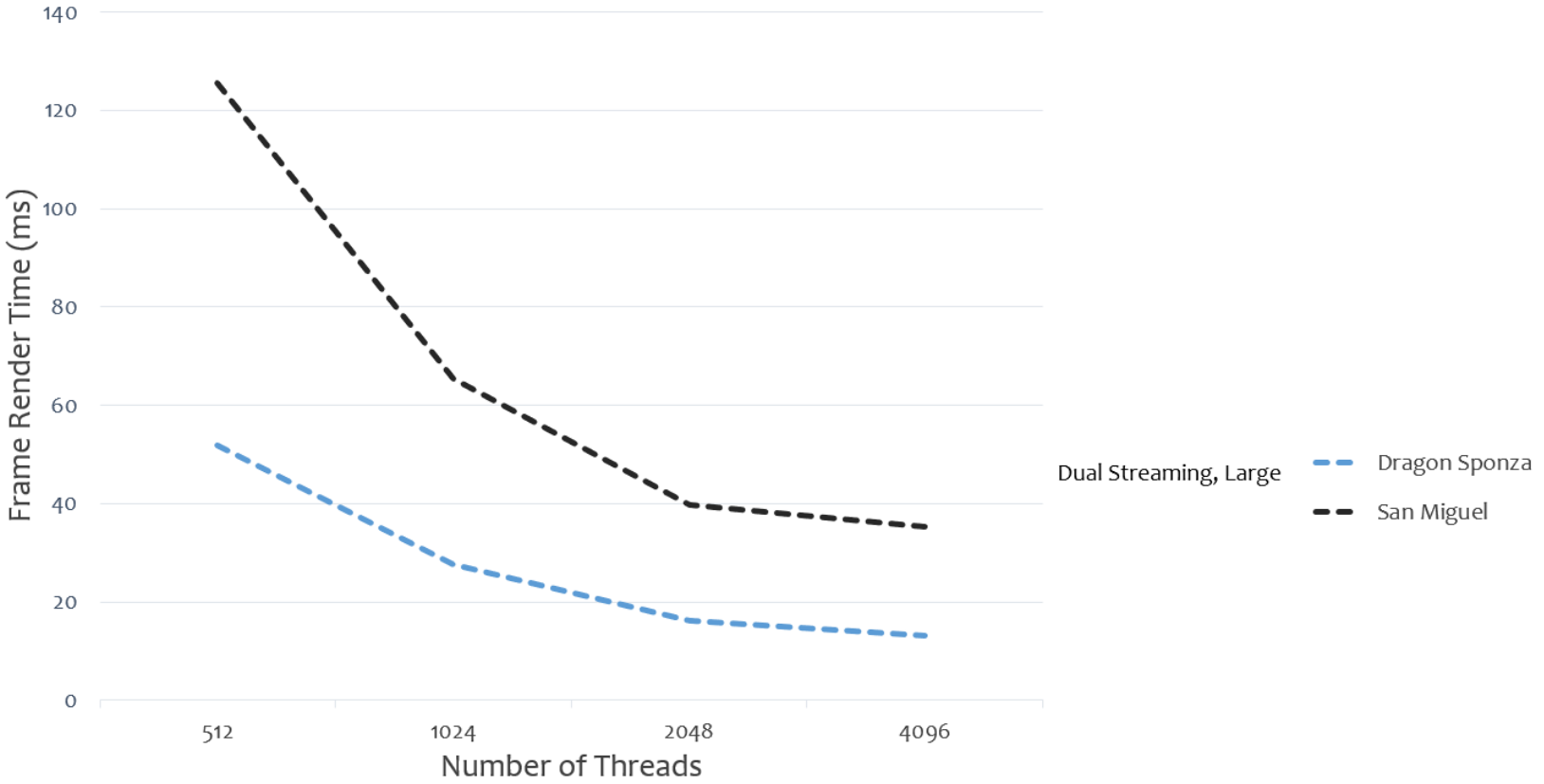
System Configuration

	MACH_RT
Frequency	2.0GHz
Threads	512/chip
DRAM bandwidth	512GB/s
L3 cache	64MB
On chip Memory	114MB

Single Large Chip



Single Large Chip: Render Time



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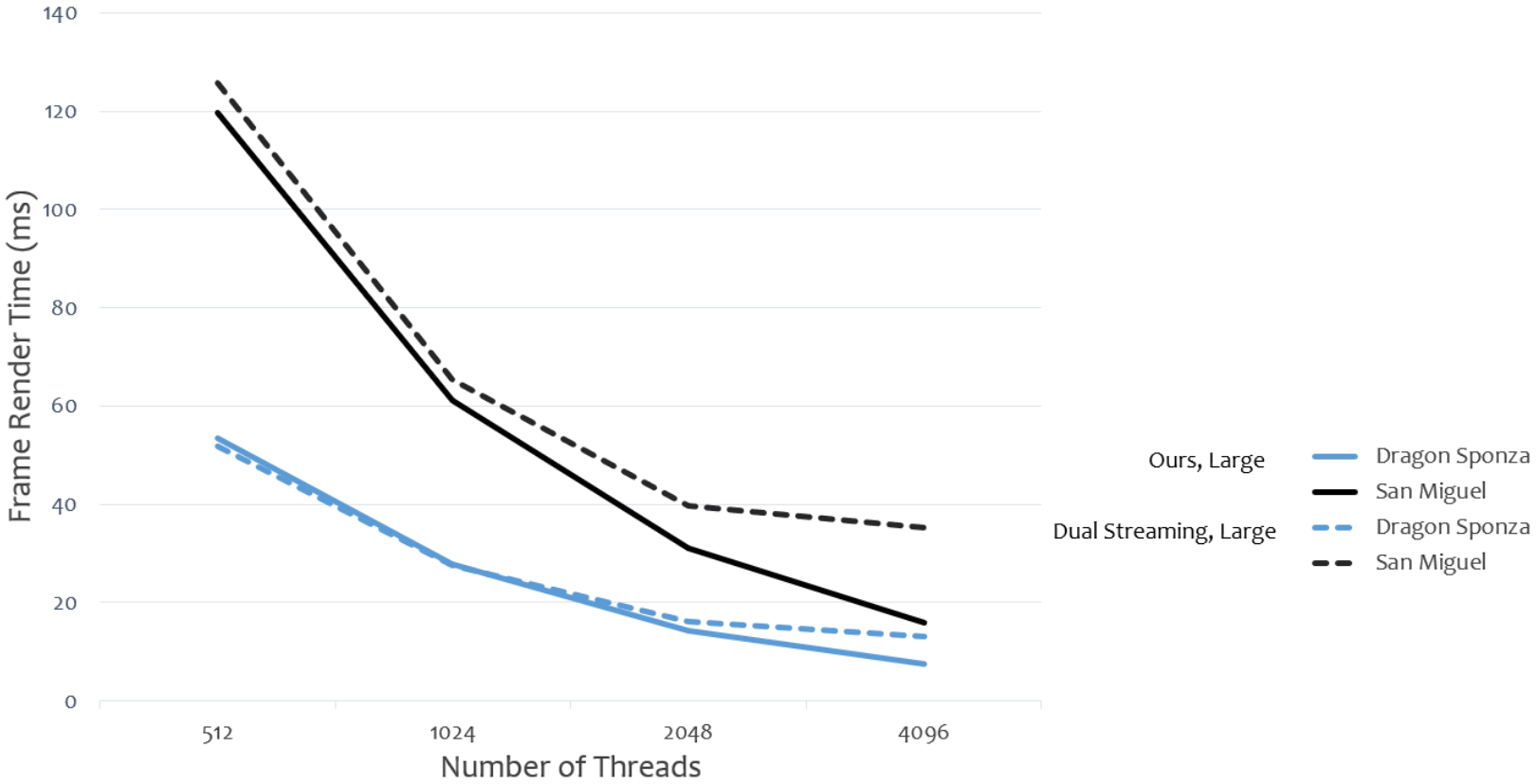
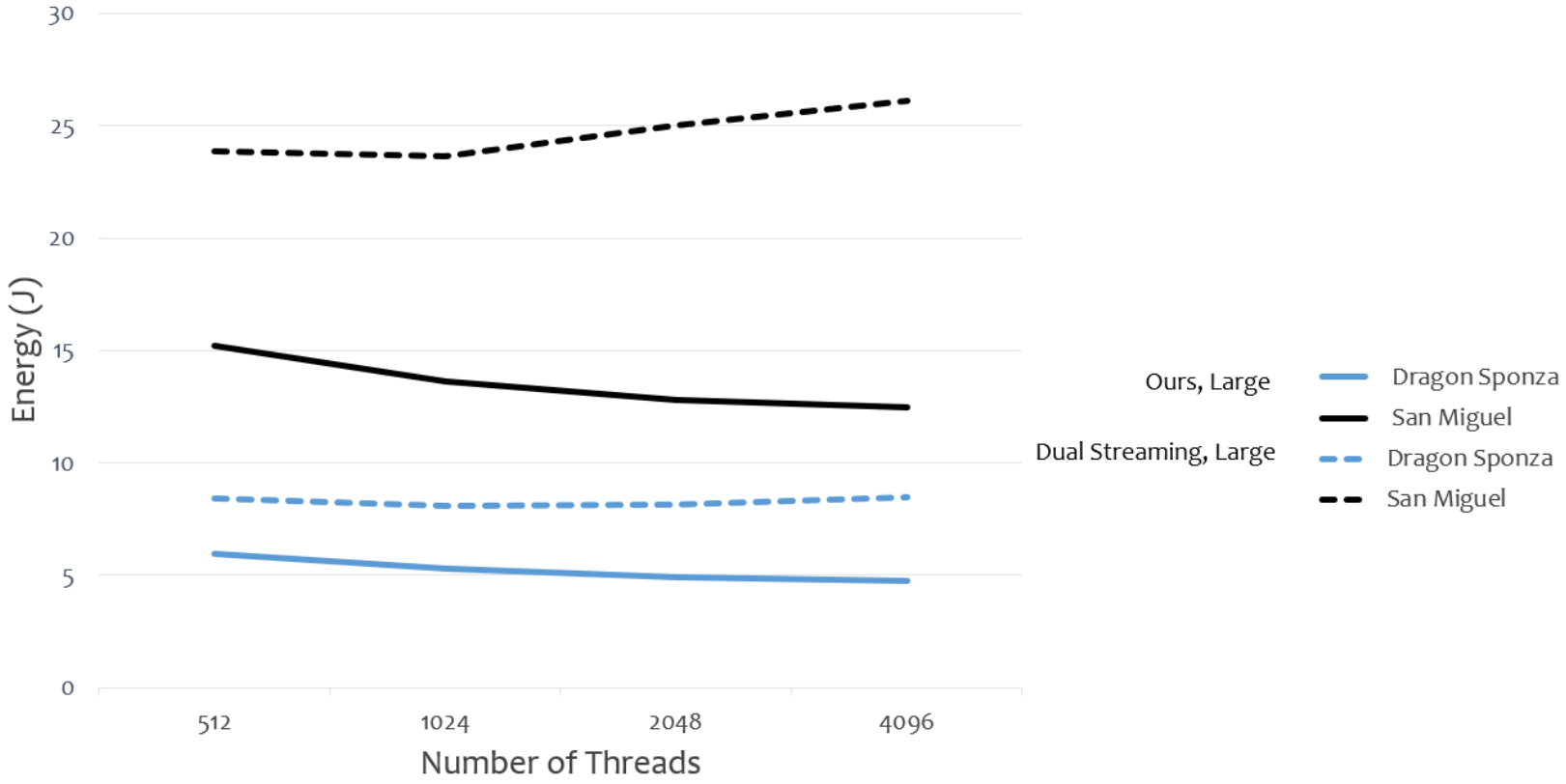
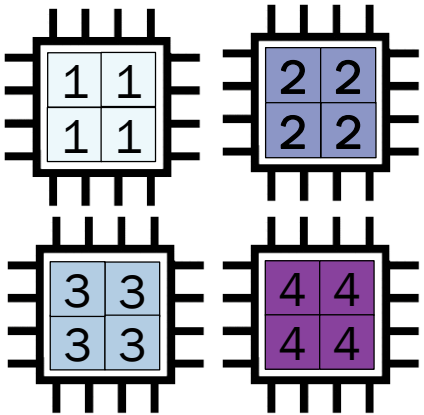


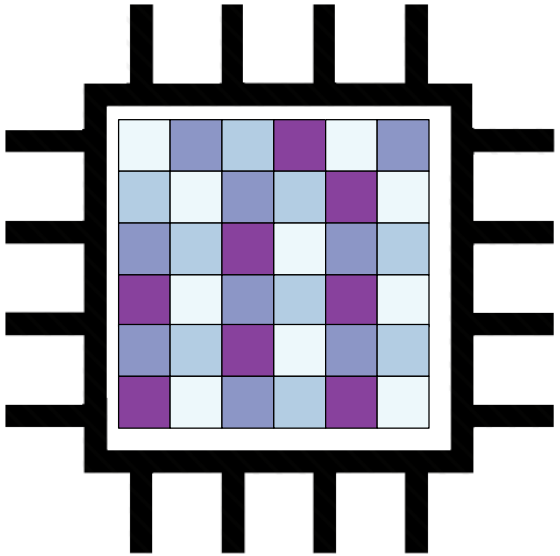
Single Large Chip: Energy



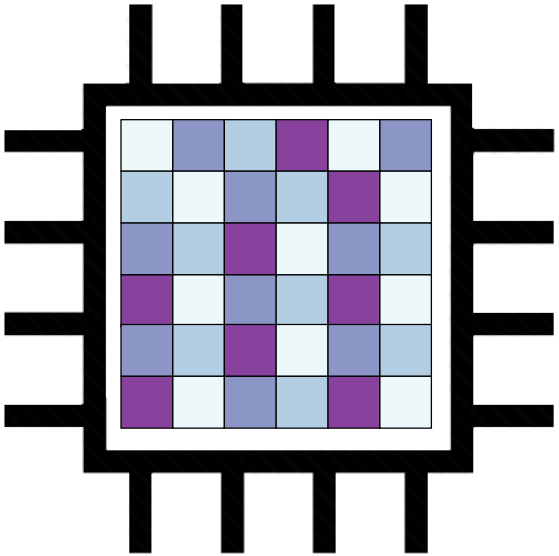
Multiple Chips



Ours



Dual Streaming
[Skhurko et al. 2017]

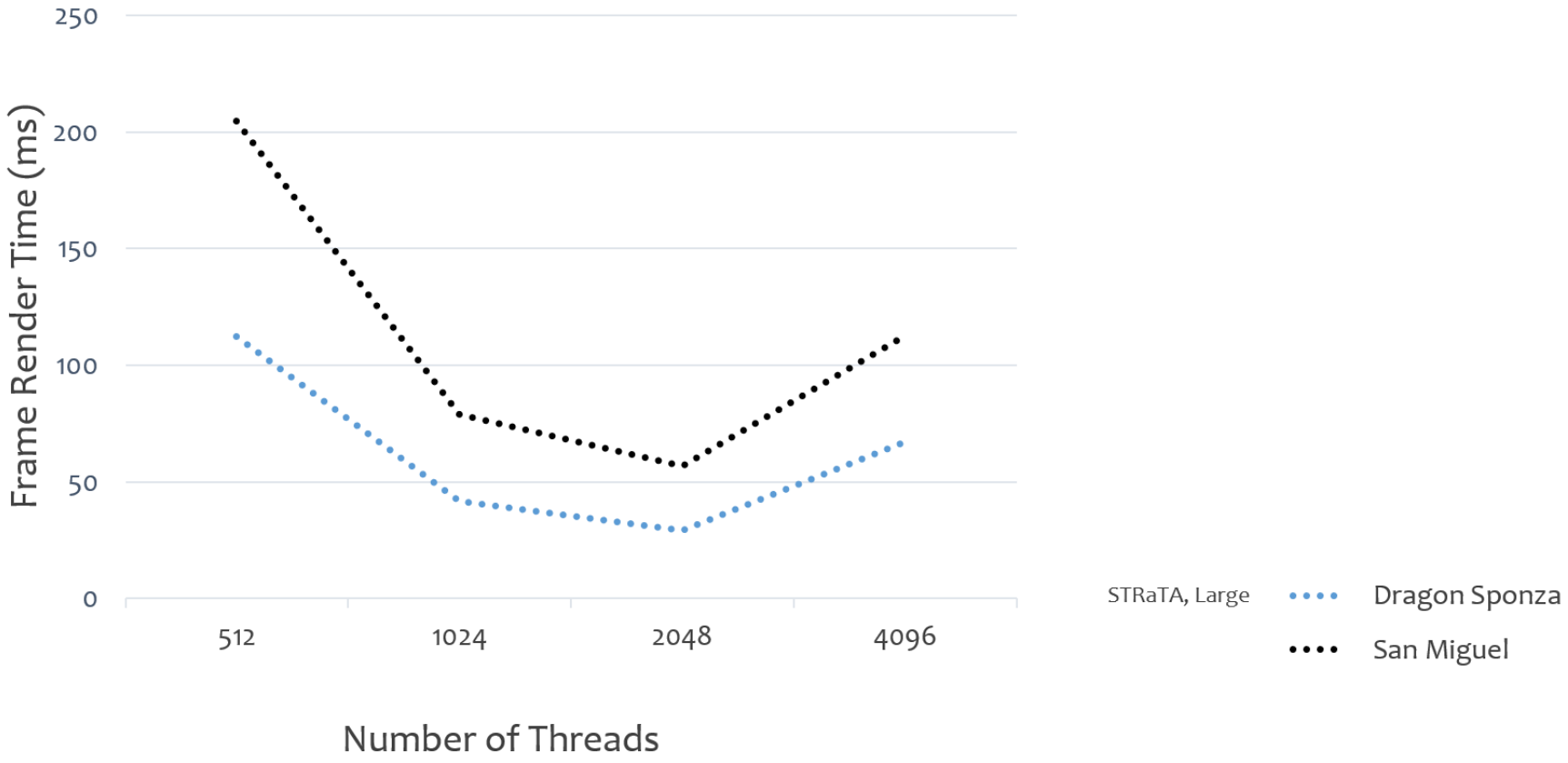


STRaTA
[Kopta et al. 2013]

STRaTA

- Energy and Bandwidth efficient
- Limited on chip ray queues
- Reconfigurable pipelines

Multiple Chips: Render Time



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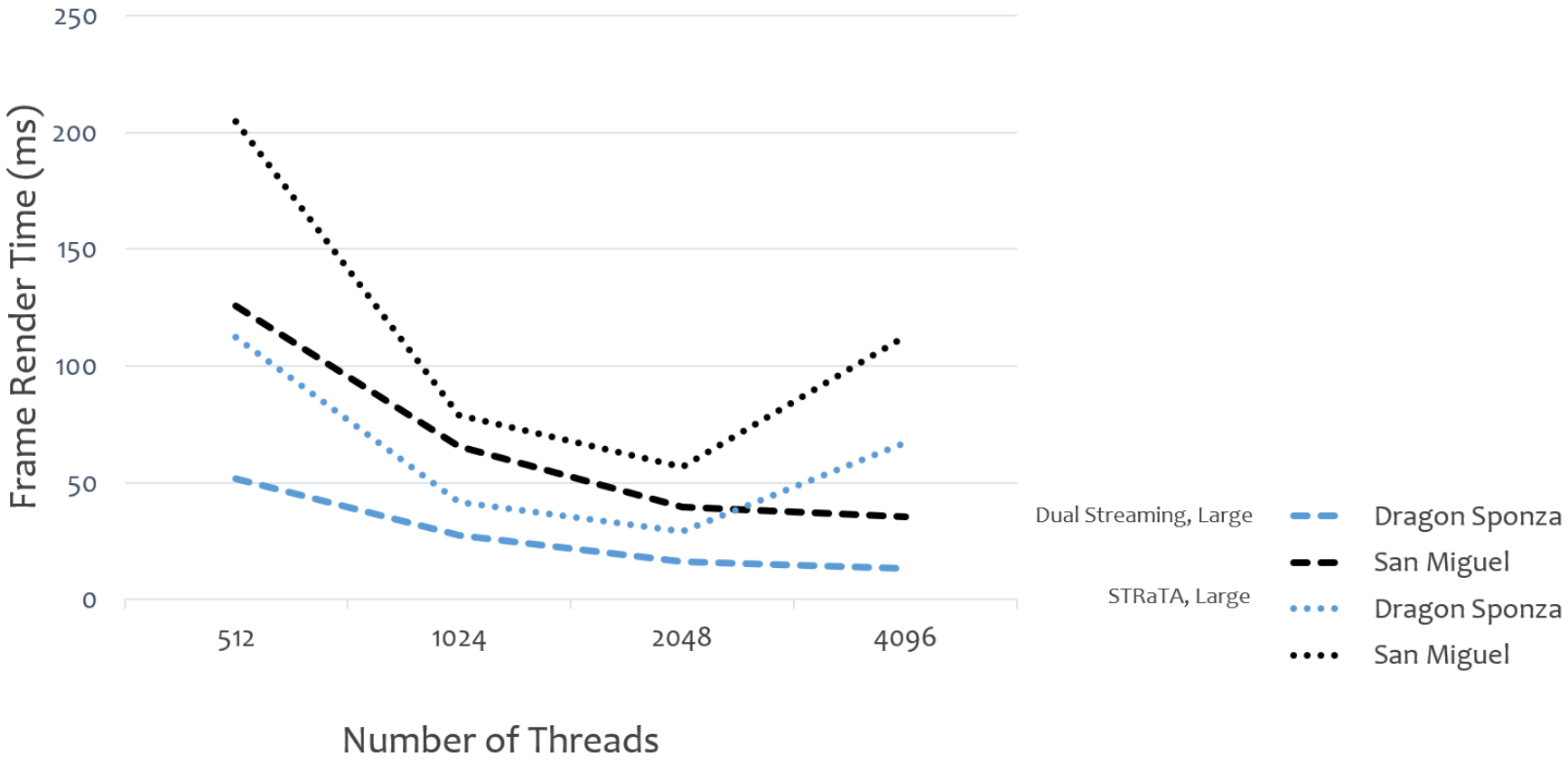

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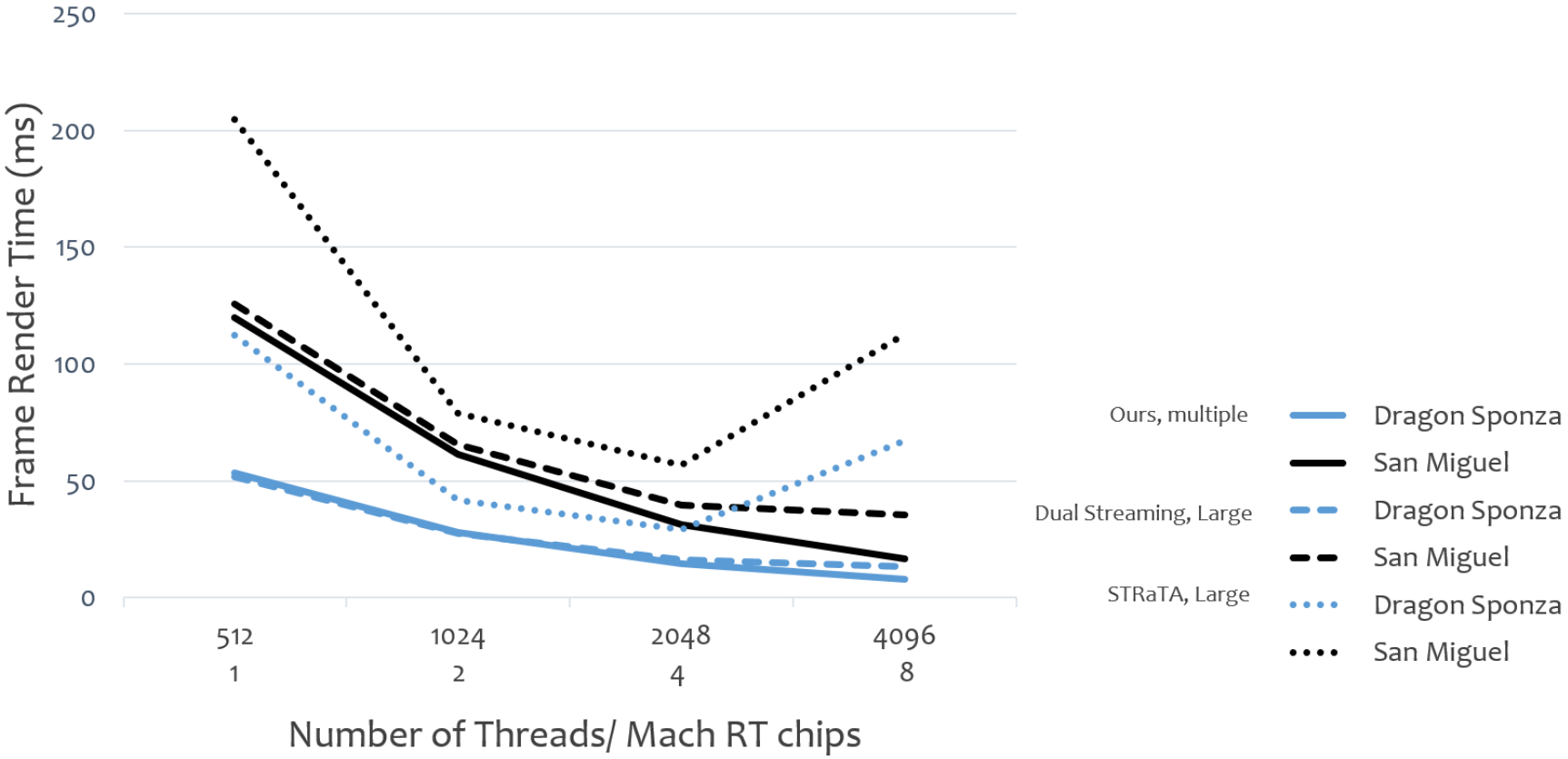
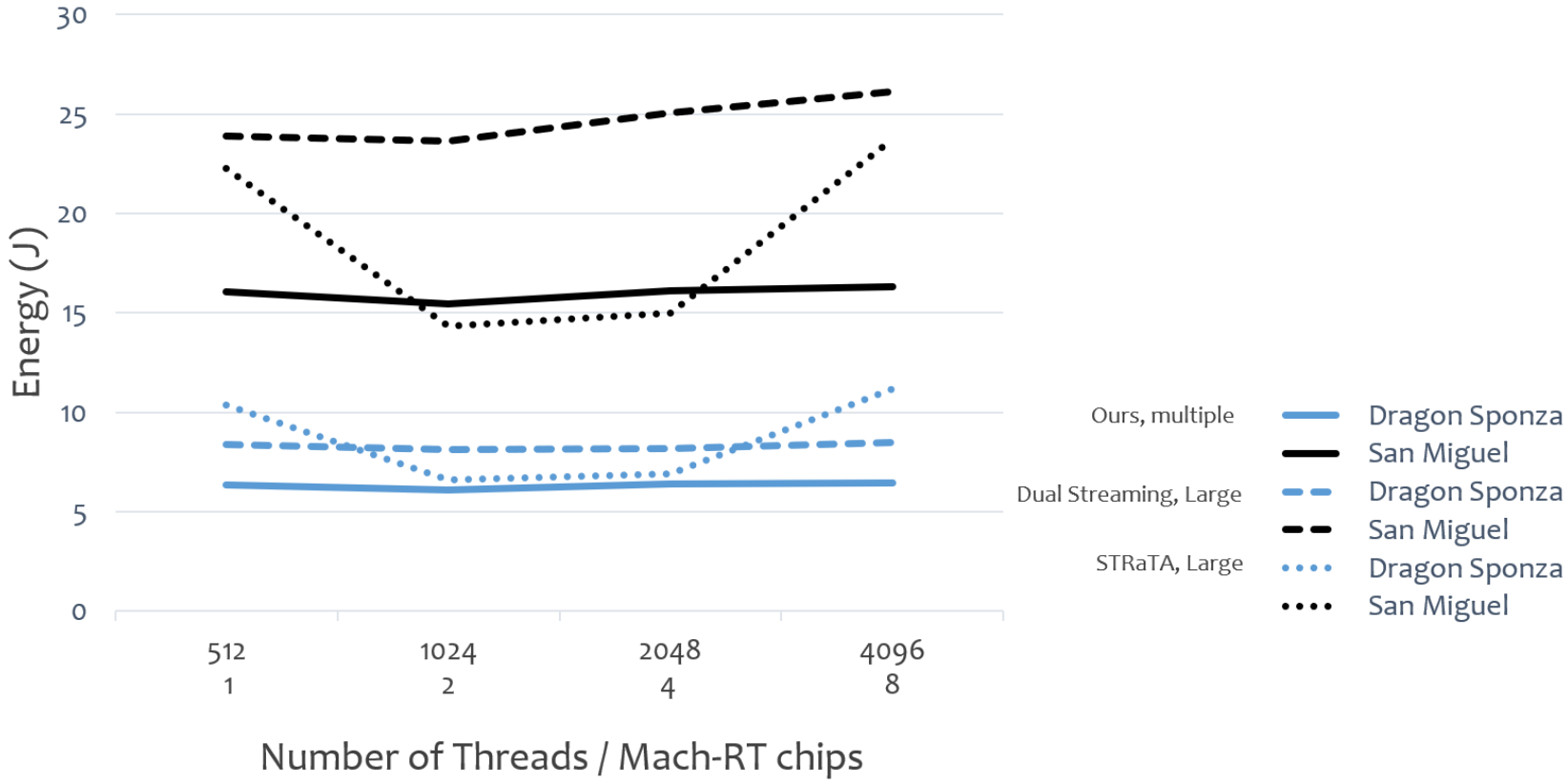
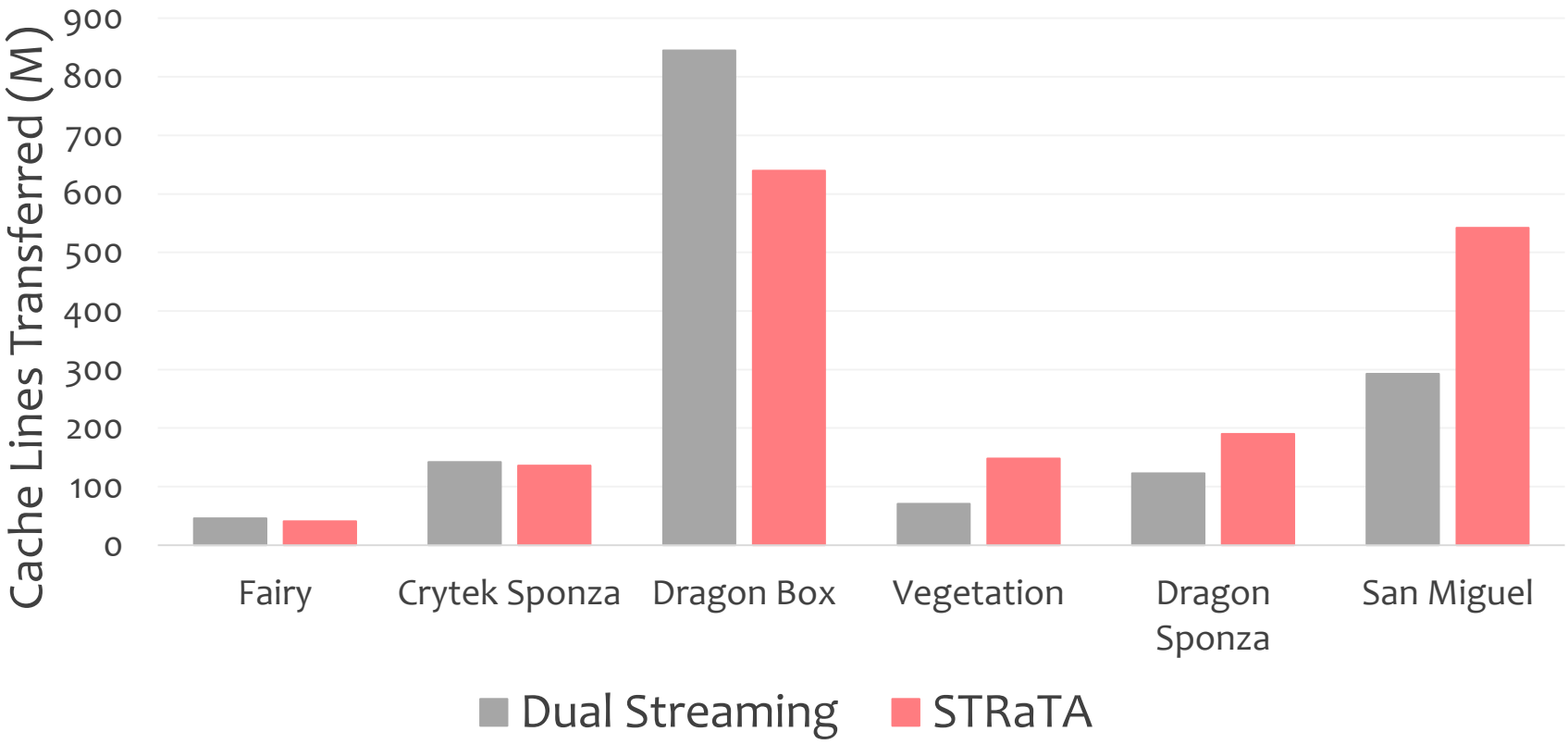


Multiple Chips: Energy



Cache Lines Transferred



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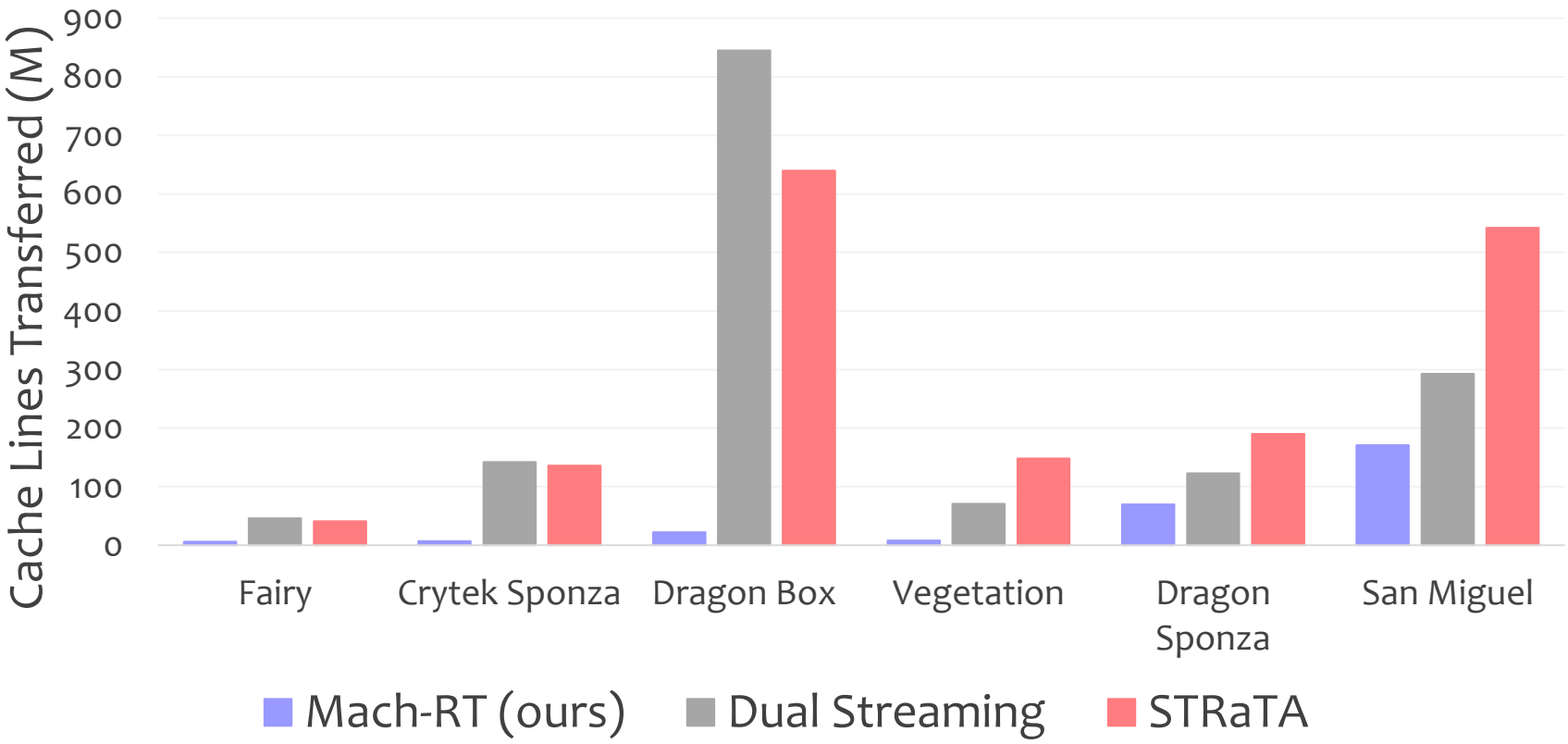
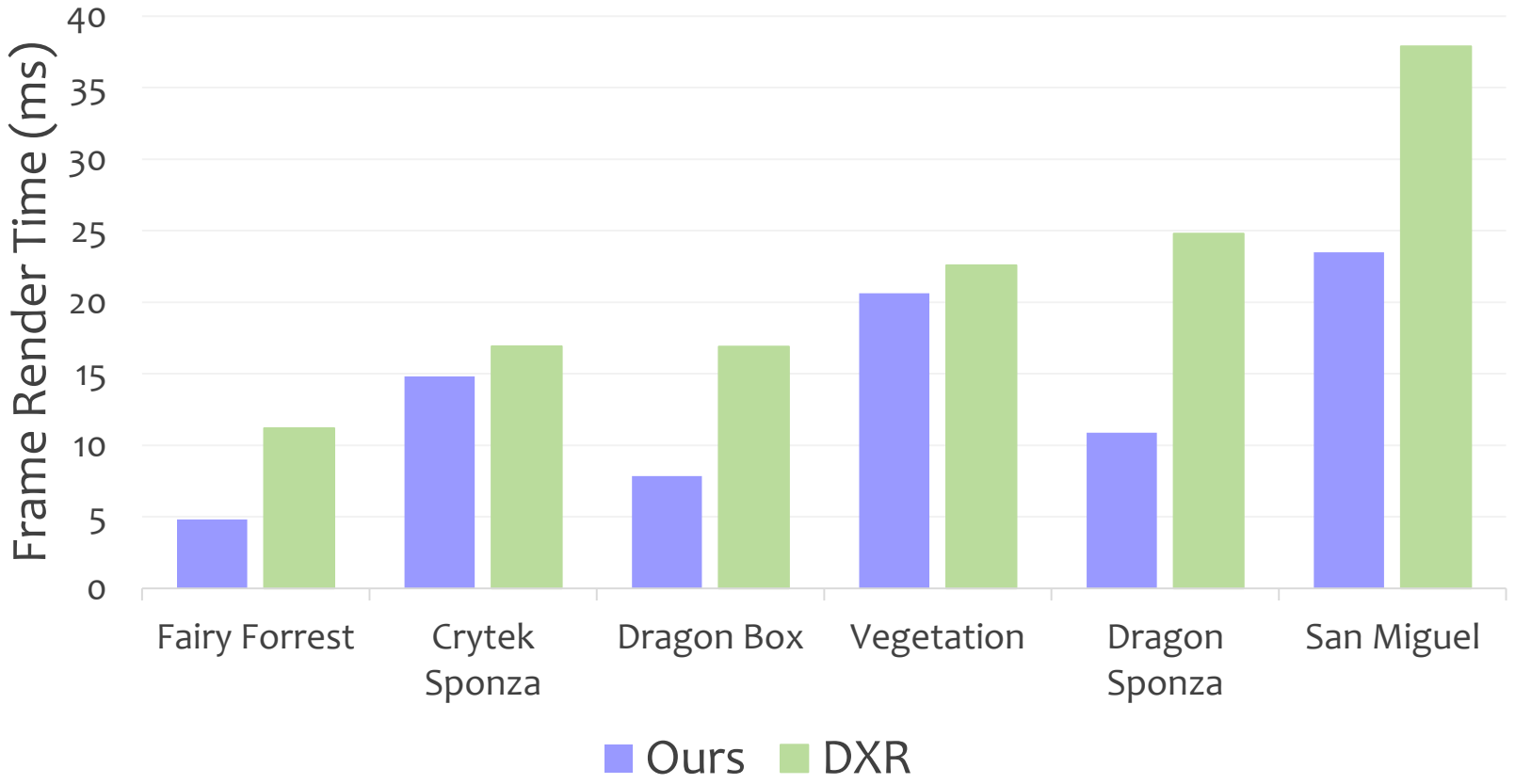


Comparisons to DXR



16 Chips

- Reduced gains
  - Work starvation
  - Large impact of scene fetches

Conclusion

- Multiple chip architecture for ray tracing
  - Is doable by using Dual Streaming
  - No ray traffic to DRAM

Q&A

Thank you!