Xe Architecture

Scaling from 10W to 500W

Alchemist GPU

Challenges

- Scaling of Xe Architecture across segments
  - Maintain a single IP
    - ~30x Range in TFs[1] & ~50x Range in power[1]
      - 10W to 500W
      - 2TFs to 60TFs
    - Varied capabilities / optimization points
- Scalable Slice Architecture
  - Scalable Xe-Cores
  - Efficiency in balancing resources

[1] *Example, Varies on final product, process technology choice*

Xe HPG

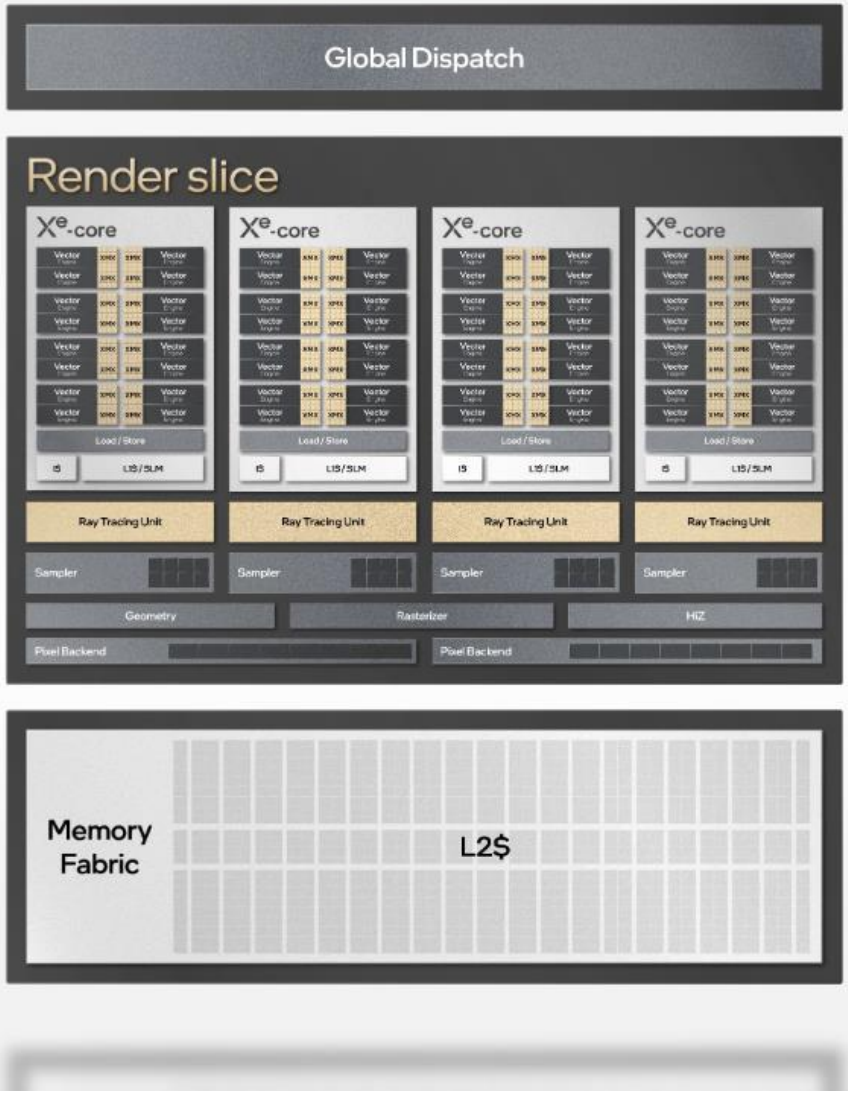
Scaling the Graphics Engine

Xe-Cores with XMX

Ray Tracing Units
Ray Traversal
Bounding Box Intersection
Triangle Intersection

Fixed Function
Optimized for DX12 Ultimate

Unified L2$
High BW, Low Latency



Scale w/ Additional Render Slices

Render Slice

4 Xe-cores with XMX

4 Ray Tracing Units

- Ray Traversal
- Bounding Box Intersection
- Triangle Intersection

Fixed Function optimized for DX12 Ultimate Gaming

Xe-core

Compute Building Block of Xe HPG-based GPUs

16
Vector Engines

256 bit
per engine

16
Matrix Engines

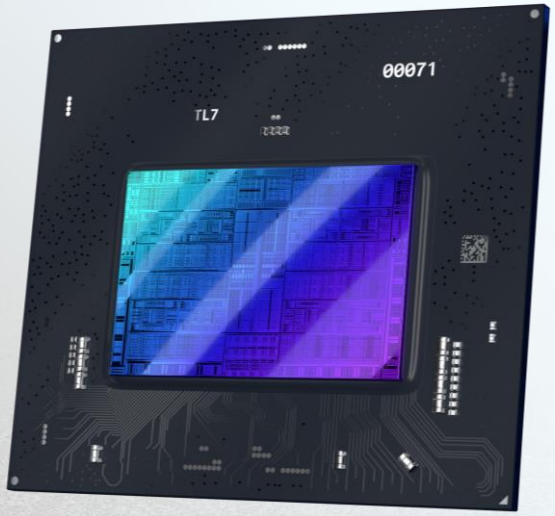
1024 bit
per engine

Multi-Year **d-GPU Road**

Performance

Alchemist

Xe HPG



Battlemage

Xe2 HPG

Celestial

Xe3 Architecture

Druid

Xe Next Architecture

intel® ARC™

intel.

THE FUTURE – EFFICIENT SOLUTIONS REQUIRE EXPLORATION

One IP

LP (iGFX)	HPG (dGFX)	HPC (DataCenter)
• Low Power (6 – 30W) • Content Creation, ML	• High Power (100 – 500W) • Path trace, Neural Rendering	• High Density OPs • HPC, AI, ML

Continue the One IP

Balance of machine for optimum raw performance, performance/W, performance/mm2.

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